

IN THE CLAIMS:

The status of each claim that has been introduced in the above-referenced application is identified in the ensuing listing of the claims. This listing of the claims replaces all previously submitted claims listings.

1. (Currently amended) A method for fabricating a chip-scale package, comprising:
positioning a preformed polymeric film over a semiconductor device with including at least one aperture that extends substantially longitudinally therethrough said preformed polymeric film aligned over a semiconductor device with the at least one aperture in substantial alignment with a corresponding bond pad of saidthe semiconductor device; and introducing conductive material into saidthe at least one aperture following the positioning.
2. (Currently amended) The method of claim 1, further comprising adhering saidthe preformed polymeric film to saidthe semiconductor device.
3. (Currently amended) The method of claim 1, further comprising defining said at least one-another aperture through saidthe preformed polymeric film.
4. (Withdrawn and currently amended) The method of claim 3, wherein said defining is effected after said positioning.
5. (Currently amended) The method of claim 3, wherein said defining is effected before said positioning.
6. (Currently amended) The method of claim 1, wherein said introducing comprises bonding saidthe conductive material to saidthe corresponding bond pad.

7. (Currently amended) The method of claim 1, wherein said introducing comprises depositing saidthe conductive material onto saidthe preformed polymeric film and within saidthe at least one aperture.

8. (Currently amended) The method of claim 7, wherein said depositing comprises chemical vapor depositing or physical vapor depositing saidthe conductive material.

9. (Withdrawn and currently amended) The method of claim 1, wherein said introducing comprises placing a preformed conductive structure within saidthe at least one aperture.

10. (Canceled)

11. (Canceled)

12. (Currently amended) The method of claim 1, further comprising forming at least one contact at an end of saidthe conductive material, opposite saidthe semiconductor device.

13. (Currently amended) The method of claim 12, further comprising placing a conductive structure adjacent saidthe at least one contact.

14. (Currently amended) The method of claim 13, wherein said placing comprises applying solder to saidthe at least one contact.

15. (Currently amended) The method of claim 1, further comprising positioning at least one conductive trace on saidthe preformed polymeric film and in communication with saidthe conductive material.

16. (Currently amended) The method of claim 15, further comprising forming at least one contact in communication with saidthe conductive trace.

17. (Currently amended) The method of claim 16, further comprising placing a conductive structure adjacent saidthe at least one contact.

18. (Currently amended) The method of claim 17, wherein said placing comprises applying solder to saidthe at least one contact.

19. (Currently amended) The method of claim 1, further comprising placing saidthe preformed polymeric film on at least a portion of a peripheral edge of saidthe semiconductor device.

20. (Currently amended) The method of claim 17, further comprising placing polymeric material at least laterally adjacent saidthe conductive structure.

21. (Original) The method of claim 17, further comprising placing a conductive elastomer over at least one conductive structure.

22. (Currently amended) The method of claim 21, further comprising placing another conductive structure in contact with saidthe conductive elastomer, opposite saidthe at least one conductive structure.

23. (Withdrawn and currently amended) A method for fabricating a chip-scale package, comprising:

placing photoimageable polymeric material on a surface of a semiconductor device; forming a polymeric film from saidthe photoimageable polymeric material with at least one aperture extending substantially longitudinally through saidthe polymeric film, saidthe at least one aperture aligned with a corresponding bond pad of saidthe semiconductor device; and

introducing conductive material into saidthe at least one aperture.

24. (Withdrawn and currently amended) The method of claim 23, wherein said forming comprises selectively exposing regions of saidthe photoimageable polymeric material to electromagnetic radiation.

25. (Withdrawn and currently amended) The method of claim 23, further comprising defining saidthe at least one aperture through saidthe polymeric film.

26. (Withdrawn and currently amended) The method of claim 25, wherein said defining is effected after saidthe forming.

27. (Withdrawn and currently amended) The method of claim 25, wherein said defining is effected substantially simultaneously with saidthe forming.

28. (Withdrawn and currently amended) The method of claim 23, further comprising placing at least one conductive trace on saidthe polymeric film and in communication with saidthe conductive material.

29. (Withdrawn and currently amended) The method of claim 28, further comprising placing at least one contact in communication with saidthe at least one conductive trace.

30. (Withdrawn and currently amended) The method of claim 29, further comprising placing at least one conductive structure adjacent saidthe at least one contact.

31. (Withdrawn and currently amended) The method of claim 30, further comprising placing polymeric material at least laterally adjacent saidthe at least one conductive structure.

32. (Withdrawn and currently amended) The method of claim 30, further comprising placing a conductive elastomer over saidthe at least one conductive structure.

33. (Withdrawn and currently amended) The method of claim 32, further comprising placing at least one other conductive structure in contact with saidthe conductive elastomer, opposite saidthe at least one conductive structure.

34. (Withdrawn and currently amended) The method of claim 23, wherein said forming comprises forming saidthe polymeric film so as to extend at least partially over a peripheral edge of saidthe semiconductor device.